**Logisim simulation screen shot:**

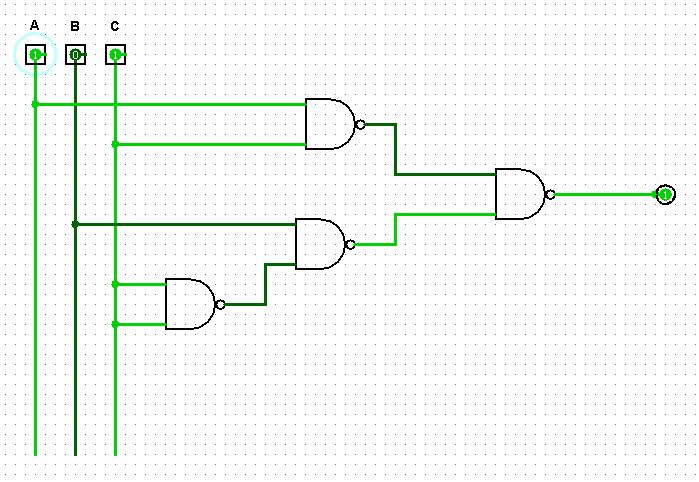
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Figure: Logisim circuit schematic of Universal (NAND) gate implementation of the circuit of Figure D2

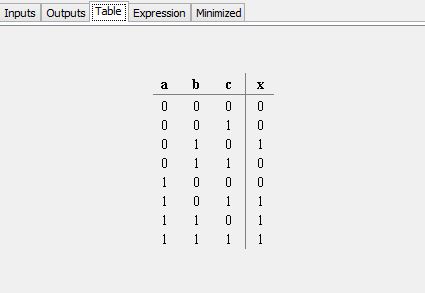
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Figure: Truth table of Universal (NAND) gate implementation of the circuit of Figure D2

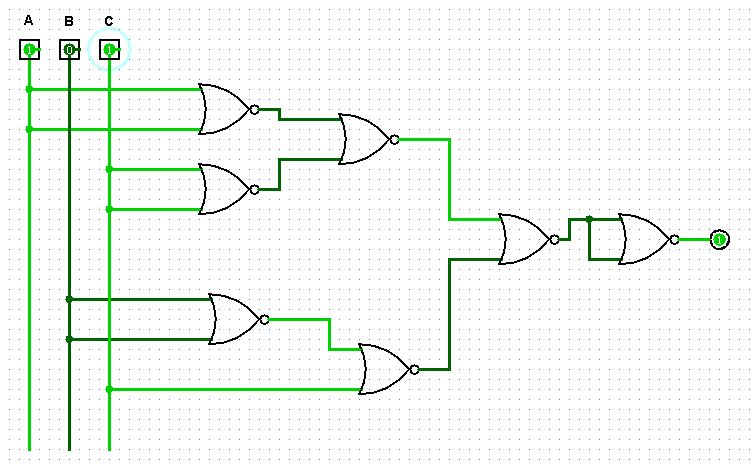
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Figure: Logisim circuit schematic of Universal (NOR) gate implementation of the circuit of Figure D2

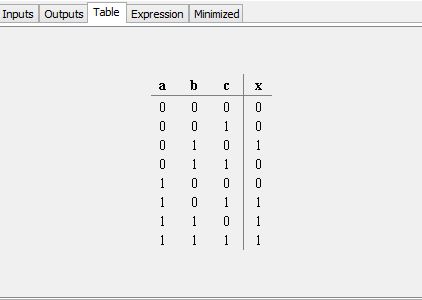
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Figure: Truth table of Universal (NOR) gate implementation of the circuit of Figure D2